REMARKS

Claims 40-58 and 70 are pending in the application with claims 40, 48, and 56 amended herein and new claim 70 added herein.

Claims 40-58 stand rejected under 35 U.S.C. 112, first paragraph, as lacking a written description in the specification. Applicant requests reconsideration.

Page 2 of the Office Action alleges that the specification does not support the first conductive lines being electrically isolated from the second conductive lines. Claims 48 and 56 are amended herein removing such limitation. Claim 40 retains the limitation and Applicant asserts that such limitation is adequately supported. Since the Office Action alleges that the present specification does not support electrical isolation of the shielding, the Office must be of the opinion that the shielding is inherently electrically connected to the shielding. Such a conclusion contradicts the express and implied teachings of the present specification, as established below.

Ground 1. Page 2, lines 1-15 of the present specification discusses the problem of cross-talk in the context of capacitive coupling. Specifically, given two closely spaced interconnect lines, a fast voltage change on a first line can undesirably cause the second line to follow the first, causing an upset "in circuits tied to the second line." The remainder of the present specification sets forth various cross-talk shielding configurations to resolve the problem of coupled voltage changes in interconnect lines. Fig. 6 shows one example. Applicant asserts that the present specification implies to those of ordinary skill that the cross-talk shielding, such as in claim 40, may be electrically

isolated from the interconnect lines that it protects. Otherwise, the voltage change induced in the cross-talk shielding by capacitive coupling might cause upset in circuits "tied" to the shielding. If the cross-talk shielding is electrically connected to the interconnect lines that the shielding is intended to protect, as implied in the Office Action, then capacitive coupling in the cross-talk shielding may upset the circuits containing the interconnect lines. Thus, the Office's allegation that the present specification does not describe the first conductive lines being electrically isolated from the second conductive lines yields the inherent conclusion that they are electrically connected. However, such an electrical connection may frustrate the providing of cross-talk shielding, which is required in the integrated circuitry claim 40. At least for such reason, the present specification must be considered to support electrical isolation of the first and second conductive lines.

Ground 2. In addition, page 10, lines 11-13 (referring to the two embodiments at page 9, lines 14-17) states that the cross-talk shielding may be connected to a suitable potential. It is clearly implied to those of ordinary skill that the cross-talk shielding is electrically isolated from the circuitry that it protects, otherwise, the applied potential would undesirably be present in the other circuitry and may upset its proper function. At least for such additional reason, the present specification must be considered to support electrical isolation of the first and second conductive lines.

Ground 3. Further, those of ordinary skill recognize the well-known practice of grounding cross-talk shielding in shielded cables. In this manner,

coupled voltage changes merely transmit to ground. Those of ordinary skill recognize that this practice requires electrical isolation of the cable conductor from the cable shielding. Accordingly, since the present specification describes providing cross-talk shielding, those of ordinary skill would appreciate that such shielding might be grounded and thus electrically isolated. At least for such further reason, the present specification must be considered to support electrical isolation of the first and second conductive lines.

Even though Applicant acknowledges the conventional practice of electrically isolating cross-talk shielding, such limitation in claim 40 nevertheless distinguishes claim 40 from the cited art. None of the references presently relied upon disclose or suggest cross-talk shielding. Instead, the Office relies upon such references for their disclosure of integrated circuitry that allegedly inherently provides cross-talk shielding. Since electrical isolation of integrated circuitry contravenes the fundamental purpose of the references, the cited art fails to disclose or suggest first conductive lines being electrically isolated from second conductive lines. Accordingly, the subject limitation in claim 40 distinguishes the relied upon references.

At least for the three grounds discussed above, Applicant asserts that the present specification supports electrical isolation of the first and second conductive lines and requests withdrawal of the lack of written description rejection in the next Office Action. Any response to Applicant's arguments should address each of the indicated three grounds.

Page 2 of the Office Action also alleges that the present specification does not support the electrically insulative oxide material on and in contact with respective first series conductive lines, as set forth in claim 56. Page 7, lines 4-12 discuss the formation of first insulating material 18 which is shown in Fig. 6 as "on and in contact with" first conductive lines 19, 20, and 21. Lines 9-12 of page 7 set forth that first insulating material 18 may predominately comprise SiO_2. Since SiO_2 is an electrically insulative oxide material, the present specification adequately supports the claim 56 electrically insulative oxide material being on and in contact with respective first series conductive lines. Applicant requests withdrawal of the lack of written description rejection in the next Office Action.

Page 2 of the Office Action further alleges that the present specification does not support individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with electrically insulative oxide material over the respective individual first series conductive lines, as set forth in claim 56. Applicant notes that page 7, lines 4-12 discusses the formation of sidewall spacers 30 and first insulating material 18. Fig. 6 clearly shows sidewall spacers 30 "connected with" first insulating material 18, which may be an electrically insulative oxide material. Accordingly, the present specification adequately supports the claimed limitation. Applicant requests withdrawal of the lack of written description rejection in the next Office Action.

At least for the reasons discussed above, Applicant requests withdrawal of the lack of written description rejection in the next Office Action.

Claims 40-55 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lur in view of Choe. Applicant requests reconsideration.

Amended claim 40 sets forth integrated circuitry including, among other features, a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another and intervening insulating spacers laterally between the first and second conductive lines. The first and second conductive lines have respective line tops and the spacers have respective spacers tops that are substantially coplanar with one or more of the first and/or second conductive line tops. The first conductive lines are electrically isolated from the second conductive lines. The series of first conductive lines or the series of second conductive lines provide cross-talk shielding for the other series.

Pages 3-4 of the Office Action allege that Lur discloses every limitation of claim 40 except for insulating spacers, electrically isolated first and second conductive lines, and providing cross-talk shielding and allege that Choe discloses the insulating spacers. Page 4 of the Office Action alleges it would be obvious to use insulating spacers to electrically isolate the lines such that cross-talk shielding is provided. The motivation for modifying Lur is alleged as providing "protection for the device, and in order to use the device in an application which requires crosstalk shielding." Applicant traverses.

Ground 1. Page 3 of the Office Action alleges that first electrode metal layer 40 discloses the claimed series of alternating first and second conductive lines. However, the Office Action does not specify what structures of Lur allegedly disclose or suggest the claimed intervening insulating

spacers. Since no express disclosure of such limitation exists in Lur, Applicant may only guess the Office's intention.

Applicant acknowledges that oxide layer 42 is shown formed over electrode metal layers 40. To the extent that the Office relies upon oxide layer 42 as disclosing or suggesting the claimed intervening insulating spacers, Applicant notes that oxide layer 42 does not include any spacer tops that are substantially coplanar with one or more of electrode metal layers 40. Thus, oxide layer 40 does not disclose the claimed intervening insulating spacers.

Also, Applicant acknowledges the presence of spacers associated with polysilicon conductors 24, which function as transistor gates. However, such spacers are not disclosed or suggested as being associated with electrode metal layers 40. To the extent that the Office relies upon the spacers associated with polysilicon conductors 24 as disclosing the claimed intervening insulating spacers, Applicant notes that such spacers are not laterally between electrode metal layers 40.

To the extent that the Office relies upon modification of Lur, Applicant asserts that no suggestion or motivation exists to modify Lur by forming the spacers of polysilicon conductor 24 on electrode metal layers 40. Polysilicon conductor 24 functions as a transistor gate while electrode metal layer 40 functions as an electrode connected by contact stud 26 to polysilicon conductor 24. The spacers associated with polysilicon conductor 24 leave the top of polysilicon conductor 24 exposed, allowing electrical connection through contact stud 26 to electrode metal layer 40. In contrast, as stated in

column 3, lines 57-68 of Lur, oxide layer 42 "surrounds all the electrode metal and inter-level metal studs" so as to protect them during etching with a solution highly selective to nitride. In such manner, electrode metal layers 40 are unaffected during the etching since they are protected by oxide layer 42. Accordingly, no suggestion or motivation exists to replace oxide layer 42 with the spacers of polysilicon conductor 24 since it would leave electrode metal layers 40 exposed.

To the extent that the Office relies upon modifying Lur by adding spacers 5, such as shown in Fig. 11A of Choe, Applicant asserts that such modification does not produce the claimed device. Applicant notes that Choe does not disclose or suggest any spacers having respective spacer tops that are substantially coplanar with one or more of the first and/or second conductive line tops, as set forth in claim 40. In fact, Choe does not disclose or suggest spacers having respective spacer tops that are substantially coplanar with any conductive line tops. Throughout Choe, the tops of gate electrodes 3 are consistently shown as not being substantially coplanar with any of the tops of spacers 5. Accordingly, Choe fails to disclose or suggest the indicated limitation and so does Lur.

At least for such reasons, Lur in view of Choe fails to disclose or suggest the intervening insulating spacers laterally between the first and second conductive lines and having respective spacer tops that are substantially coplanar with one or more of the first and/or second conductive line tops, as set forth in claim 40.

Ground 2. Claim 40 additionally sets forth that the first conductive lines are electrically isolated from the second conductive lines. Page 3 of the Office Action acknowledges that Lur fails to disclose this limitation. Page 4 of the Office Action states that it would be obvious to use spacers 5 of Choe to electrically isolate the first and second conductive lines. However, column 4, lines 6-26 and elsewhere throughout Lur state that electrode metal layers 40 are part of a very large scale integrated circuit. Electrode metal layers 40 are interconnected to transistor gates (polysilicon conductors 24) through contact studs 26. Those of ordinary skill readily recognize that electrode metal layers 40 such as shown in Fig. 11 of Lur cannot be electrically isolated from one another, as set forth in claim 40, and still function as intended. Simply by forming part of an integrated circuit, electrode metal layers 40 are necessarily electrically connected. Accordingly, Applicant asserts that Lur fails disclose the indicated limitation of claim 40.

Since page 4 of the Office Action also refers to Choe in the allegation regarding disclosure of electrically isolated conductive lines, Applicant notes that Choe also fails to disclose the indicated limitation of claim 40. Specifically, gate electrodes 3 shown in Fig. 11A of Choe are described throughout the reference as being part of memory cells within a memory device. Since the memory device includes integrated circuitry, Choe cannot be considered to disclose or suggest gate electrodes 3 as being electrically isolated from one another. Combination of references cannot disclose or suggest subject matter that is absent from both.

Ground 3. Establishing a prima facie case of obviousness requires that the prior art teach or suggest all of the claimed limitations. Thus, as indicated above, the Office Action fails to establish a prima facie case of obviousness. A prima facie case of obviousness also requires that the prior art suggest to those of ordinary skill that they make the claimed device. Applicant acknowledges a discussion in Lur regarding reducing interelectrode parasitic capacitance by reducing the dielectric constant of dielectric material between electrodes. The entire focus in Lur for reducing parasitic capacitance involves the dielectric constant of interelectrode dielectric material. Thus, Lur uses air dielectric 85 to reduce the dielectric constant and address parasitic capacitance. Regardless of whether Lur addresses problems of parasitic capacitance, Lur fails to provide any mention of capacitive coupling or describe any solutions that address capacitive coupling. Page 1, lines 18-21 of the present specification expressly state that merely lowering the dielectric constant of insulators between conductive metal lines (as in Lur) is not expected to solve the cross-talk problem. Accordingly, the invention of claim 40 addresses the problem of capacitive coupling in a manner directly different from Lur. Lur fails to even recognize the problem of capacitive coupling.

Applicants note that the Federal Circuit has determined that the "problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem." Diversitech Corp. v. Century Steps Inc., 7 USPQ2d 1315, 1318 (Fed. Cir. 1988). If the references do not address or even recognize the

problem they cannot begin to teach or suggest a solution to it. Neither reference cited in the Office Action addresses the problem solved by Applicant's invention and, accordingly, cannot suggest a solution to such problem. The Federal Circuit further stated that "the nature of the problem 'which persisted in the art,' and the inventor's solution, are factors to be considered in determining whether the invention would have been obvious to a person of skill in that art." Northern Telecom v. Datapoint Corp., 15 USPQ2d 1321, 1324 (Fed. Cir. 1990). At least for such reason, Applicant asserts that the cited combination of references does not suggest to those of ordinary skill that they should make the claimed device. The Office Action thus fails to establish a prima facie case of obviousness at least for such additional reason.

Ground 4. Page 3 and 8 of the Office Action acknowledge that Lur does not expressly disclose providing cross-talk shielding and allege that it is inherently provided. However, "the mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency." In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (citations omitted) (emphasis in original); MPEP 2112. Further, "[i]n relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added); MPEP 2112. The Office Action fails to provide a basis in fact and/or technical reasoning sufficient to establish that Lur

inherently discloses the cross-talk shielding of claim 40. The Lur structures do not necessarily provide cross-talk shielding. It is not enough merely to show that the Lur structures might provide the claimed shielding.

Applicant herein establishes the following four grounds supporting patentability of claim 40, any one of which is sufficient: 1) both Lur and Choe fail to disclose or suggest the claimed spacer, 2) both Lur and Choe fail to disclose or suggest electrical isolation of the first and second conductive lines, 3) the prior art does not suggest making the claimed device, and 4) Lur does not inherently disclose cross-talk shielding. Any response to Applicant's arguments should address each of the indicated three grounds supporting patentability.

Claims 41-47 and 70 depend from claim 40 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 70 sets forth that the first conductive lines and the second conductive lines are electrically isolated from one another laterally solely by the spacers. Neither Lur nor Choe disclose or suggest such a limitation. Electrode metal layers 40 in Lur are electrically isolated from one another laterally by both oxide layer 42 and air dielectric 85.

Claim 48 sets forth integrated circuitry that includes, among other features, a series of alternating first and second conductive lines directly over a layer of insulating material and intervening strips of insulating material having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second

conductive lines. The first conductive lines and the second conductive lines are separated from one another laterally solely by the intervening strips of insulating material. Pages 5-6 of the Office Action allege that Lur discloses every limitation of claim 48. However, review of Lur (as well as Choe) does not reveal any disclosure or suggestion of first and second conductive lines separated from one another laterally solely by intervening strips of insulating material having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines. Accordingly, Applicant asserts that the cited references fail to disclose or suggest every limitation of claim 48. Claims 49-55 depend from claim 48 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Claims 56-58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chu in view of Miyanaga. Applicant requests reconsideration.

Amended claim 56 sets forth integrated circuitry that includes, among other features, a series of first conductive polysilicon lines over a BPSG layer, electrically insulative oxide material on and in contact with respective first series conductive lines and a top of the insulative oxide material over at least some of the first series conductive lines defining a first plane. The integrated circuitry includes a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with the first plane. Pages 6-8 of the Office Action allege that Chu in view of Miyanaga discloses every limitation of claim

56 except for electrically insulative oxide material on and in contact with respective first series conductive lines and having the structural features set forth in claim 56. The Office Action relies upon Okummura as allegedly remedying such deficiency. Applicant traverses.

Ground 1. Page 7 of the Office Action makes certain allegations regarding the teachings of Okummura and modifications of Chu. However, the Office Action does not describe the specific modification to Chu that is proposed. It appears that the Office Action alleges that gate electrode 9 in Fig. 12 of Okummura discloses the claimed series of first conductive polysilicon lines. It also appears that the Office Action proposes replacing polysilicon gates 302 and insulating layer 304 in Chu with gate electrode 9 of Okummura so that Chu's insulating layer 312 is on and in contact with gate electrode 9, as substituted into Chu. However, as stated in column 3, lines 49-50 of Chu, insulating layer 304 serves as insulation for the upper surface of memory cells 400.

As is readily apparent to those of ordinary skill, review of Figs. 3H-3O and the text associated therewith in Chu reveals that the process of forming the invention in Chu relies critically upon the presence of insulating layer 304 during subsequent processing. Chu also relies critically upon the presence of insulating layer 304 as a structural feature in the final product to protect and/or insulate polysilicon gates 302. Clearly, substituting gate electrode 9 of Okummura, which lacks an insulation layer separating gate electrode 9 from oxide layer 12, would frustrate the intended purpose or change the principle of operation of the Chu invention. Accordingly, no suggestion or motivation

may be considered to exist to make the proposed modification. At least for such reason, the cited combination of references fails to properly disclose or suggest every limitation of claim 56.

Ground 2. None of the cited references considered alone disclose or suggest the claimed second plane that is coplanar with the claimed first plane. The second plane is defined by respective line tops of a series of second conductive aluminum-containing lines. The first plane is defined by a top of the insulative oxide material over at least some of the first series of conductive polysilicon lines. Since none of the references disclose or suggest such a feature, Applicant asserts that combination of the references cannot be considered to disclose or suggest subject matter that is absent from all.

Ground 3. In addition, as established above, no motivation exists in the cited art to modify Chu in a manner that would produce the indicated limitations of claim 56. Page 7 of the Office Action provides a lengthy list of advantages that presumably provide the motivation to modify Chu's device according to the teachings of Okamura. No other motivations are alleged. However, the Office Action fails to provide any reasoning why replacing polysilicon gates 302 and insulating layer 304 in Chu with gate electrode 9 of Okummura so that Chu's insulating layer 312 is on and in contact with gate electrode 9, as substituted into Chu, provides the described advantages. Applicant asserts that such a modification of Chu does not provide any of the described advantages. As such, the motivation alleged by the Office is

invalid and does not establish the required motivation in the art to modify Chu as proposed.

Applicant herein establishes at least three grounds supporting patentability of claim 56, any one of which is sufficient: 1) Chu cannot be properly modified by Okummura, 2) none of the cited references disclose structural features that provide the claimed first plane coplanar with the second plane, and 3) the alleged motivation to combine is improper. Any response to Applicant's arguments should include a response to each of the three grounds. Claims 57 and 58 depend from claim 56 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Applicant herein establishes adequate reasons supporting patentability of claims 40-58 and 70 and requests allowance of all pending claims in the next Office Action.

Respectfully submitted,

Dated: 12 Sep 2005 By: _____

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